POWER8

Jeff Stuecheli
IBM Power Systems
IBM Systems & Technology Group Development
History...

**POWER5**
- **Technology**: 130nm SOI
- **Compute**
  - Cores: 2
  - Threads: SMT2
- **Caching**
  - On-chip: 1.9MB
  - Off-chip: 36MB
- **Bandwidth**
  - Sust. Mem.: 15GB/s
  - Peak I/O: 3GB/s

**POWER6**
- **Technology**: 65nm SOI
- **Compute**
  - Cores: 2
  - Threads: SMT2
- **Caching**
  - On-chip: 8MB
  - Off-chip: 32MB
- **Bandwidth**
  - Sust. Mem.: 30GB/s
  - Peak I/O: 10GB/s

**POWER7**
- **Technology**: 45nm SOI eDRAM
- **Compute**
  - Cores: 8
  - Threads: SMT4
- **Caching**
  - On-chip: 2 + 32MB
  - Off-chip: None
- **Bandwidth**
  - Sust. Mem.: 100GB/s
  - Peak I/O: 20GB/s

**POWER7+**
- **Technology**: 32nm SOI eDRAM
- **Compute**
  - Cores: 8
  - Threads: SMT4
- **Caching**
  - On-chip: 2 + 80MB
  - Off-chip: None
- **Bandwidth**
  - Sust. Mem.: 100GB/s
  - Peak I/O: 20GB/s
# History...

<table>
<thead>
<tr>
<th>Technology</th>
<th>POWER5 2004</th>
<th>POWER6 2007</th>
<th>POWER7 2010</th>
<th>POWER7+ 2012</th>
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<td>Peak I/O</td>
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**Today’s Topic**
## POWER8 Vision

### Leadership Performance
- Increase core throughput at single thread, SMT2, SMT4, and SMT8 level
- Large step in per socket performance
- Enable more robust multi-socket scaling

### System Innovation
- Higher capacity cache hierarchy and highly threaded processor
- Enhanced memory bandwidth, capacity, and expansion
- Flexible SMT
- Dynamic code optimization
- Hardware-accelerated virtual memory management

### Open System Innovation
- CAPI
- Memory interface
- Open system software
POWERS8 Processor

Technology
- 22nm SOI, eDRAM, 15 ML 650mm2

Caches
- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3
- Up to 128 MB eDRAM L4 (off-chip)

Memory
- Up to 230 GB/s sustained bandwidth

Bus Interfaces
- Durable open memory attach interface
- Integrated PCIe Gen3
- SMP Interconnect
- CAPI (Coherent Accelerator Processor Interface)

Cores
- 12 cores (SMT8)
- 8 dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction cache

Accelerators
- Crypto & memory expansion
- Transactional Memory
- VMM assist
- Data Move / VM Mobility

Energy Management
- On-chip Power Management Micro-controller
- Integrated Per-core VRM
- Critical Path Monitors
**POWER8 Core**

**Execution Improvement vs. POWER7**
- SMT4 → SMT8
- 8 dispatch
- 10 issue
- 16 execution pipes:
  - 2 FXU, 2 LSU, 2 LU, 4 FPU, 2 VMX, 1 Crypto, 1 DFU, 1 CR, 1 BR
- Larger Issue queues (4 x 16-entry)
- Larger global completion, Load/Store reorder
- Improved branch prediction
- Improved unaligned storage access

**Larger Caching Structures vs. POWER7**
- 2x L1 data cache (64 KB)
- 2x outstanding data cache misses
- 4x translation Cache

**Wider Load/Store**
- 32B → 64B L2 to L1 data bus
- 2x data cache to execution dataflow

**Enhanced Prefetch**
- Instruction speculation awareness
- Data prefetch depth awareness
- Adaptive bandwidth awareness
- Topology awareness

**Core Performance vs. POWER7**
- ~1.6x Single Thread
- ~2x Max SMT
POWER8 On Chip Caches

- L2: 512 KB 8 way per core
- L3: 96 MB (12 x 8 MB 8 way Bank)
- “NUCA” Cache policy (Non-Uniform Cache Architecture)
  - Scalable bandwidth and latency
  - Migrate “hot” lines to local L2, then local L3 (replicate L2 contained footprint)
- Chip Interconnect: 150 GB/sec per direction per segment
Cache Bandwidths

GB/sec shown assuming 4 GHz
- Product frequency will vary based on model type

Across 12 core chip
- 4 TB/sec L2 BW
- 3 TB/sec L3 BW
POWER8 Memory Organization

- Up to 8 high speed channels, each running up to 9.6 Gb/s for up to 230 GB/s sustained
- Up to 32 total DDR ports yielding 410 GB/s peak at the DRAM
- Up to 1 TB memory capacity per fully configured processor socket (at initial launch)
POWER8 Memory Buffer Chip …with 16MB of Cache…

Intelligence Moved into Memory
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
  - Formerly on Processor
  - Moved to Memory Buffer

Processor Interface
- 9.6 GB/s high speed interface
- More robust RAS
- “On-the-fly” lane isolation/repair
- Extensible for innovation build-out

Performance Value
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)
POWER8 Integrated PCIe Gen 3

Native PCI Gen 3 Support
- Direct processor integration
- Replaces proprietary GX/Bridge
- Low latency
- High Gen 3 bandwidth (8 Gb/s)
  (High utilization realizable)

Transport Layer for CAPI Protocol
- Coherently Attach Devices connect to processor via PCI
- Protocol encapsulated in PCI

POWER7

POWER8

I/O Bridge

GX Bus

PCI

PCI Device

POWER8

PCI

PCI Device
**POWER8 CAPI** Coherence Attach Processor Interface

**Virtual Addressing**
- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

**Hardware Managed Cache Coherence**
- Enables the accelerator to participate in “Locks” as a normal thread
- Lowers Latency over IO communication model

**Customizable Hardware Application Accelerator**
- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL

**Processor Service Layer (PSL)**
- Present robust, durable interfaces to applications
- Offload complexity / content from CAPP

**PCI Gen 3**
*Transport for encapsulated messages*

**Coherence Bus**
Socket Performance

- POWER7+ baseline
- Memory Bandwidth
- Commercial
- Java
- Integer
- Floating Point

3
2.5
2
1.5
1
0.5
0
# POWER8 Innovation

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- Industry Solutions

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  - Art of the possible

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POWER8 Enabling: …Big Data, Analytics, Cognitive Computing…

POWER8 Differentiation for Analytics
• Massive capacity bandwidth to memory
• Large caches, massive bandwidth to them
• SMT8, Many threads to hide memory latency
  – Graph traversals
  – Transactional memory enables efficient thread scaling

CAPI Accelerators
• Enables heterogeneous compute (GPU, FPGA, etc.)

Synergy with IBM Software, Driving Optimization Across the Stack
POWER8

- Significant Performance at Thread, Core, and System
- Optimization for VM Density & Efficiency
- Strong Enablement of Autonomic System Optimization
- Excellent Big Data Analytics Capability
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